IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

First Named Inventor	:	STUTTARD, Dave
Application No.	:	09/972,797
Patent No.	:	7,363,472
Issue Date	:	April 22, 2008
Art Unit	:	2183
Confirmation Number	:	3642
Examiner	:	Huisman, David J.
Title	:	Memory Access Consolidation For SIMD Processing Elements Having Access Indicators
Attorney Docket No.	:	HASE0001

November 07, 2008

Commissioner of Patents and Trademarks
Mail Stop: Certificate of Corrections Branch
P.O. Box 1450
Alexandria, VA. 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 CFR § 1.322

The enclosed Certificate of Correction (PTO/SB/44) for the above-identified patent is submitted under 37 CFR § 1.322.

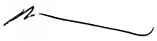
Claim 1 (formally Claim 72 during prosecution) was not amended as recorded in the Examiner's Amendment on Page 2 of the Notice of Allowability. Applicant, by his attorney, requests the following correction:

Claim 1 at column 24, line 11, replace "or each" with --at least one--.

The correction does not involve such changes in the patent as would constitute new matter or would require reexamination as set forth in 35 U.S.C. § 254. Therefore, no new matter is provided with this Certificate of Correction.

The Commissioner is hereby authorized to charge the fee set forth in 37 CFR § 1.20(a) and any additional fees due, to Deposit Account 07-1445 (Order No. HASE0001).

Respectfully submitted,



Michael A. Glenn
Reg. No. 30,176

Customer No. 22862

PTO/SB/44 (09-07)
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 7,363,472

APPLICATION NO.: 09/972,797

ISSUE DATE : April 22, 2008

INVENTOR(S) : Dave Stuttard, Dave Williams, Eamon O'Dea, Gordon Faulds, John Rhoades, Ken Cameron, Phil Atkin, Paul Winser, Russell David, Ray McConnell, Tim Day, and Trey Greer.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

1. A method of retrieving a data item from a memory unit in a data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, wherein the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items and wherein the data processing apparatus includes said memory unit in which data items are stored at addresses therein, and to which the plurality of processing elements have access, the method comprising: for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required; selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element; transmitting the retrieved target address and transaction identification information to the processing elements in the array; for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and it the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information; retrieving at least one data item stored at the transmitted target address in the memory unit; transmitting the at least one retrieved data item and associated transaction identification information to the processing elements in the array; and for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, receiving the at least one retrieved data item.

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GLENN PATENT GROUP
3475 EDISON WAY, SUITE L
MENLO PARK, CA 94025

is input into the PE register file **1061***b*. When the transaction ID is returned to the processing block, the processing elements compare the stored transaction ID with the incoming transaction ID, in order to recover the data.

Using transaction IDs in place of simply storing the accessed address information enables multiple memory accesses to be carried, and then returned in any order.

Booth multiplication is achieved using the B multiplexer **212**, which is shown in more detail in FIG. **14**. The B multiplexer **212** receives inputs **230** from the V and P registers and from the MEE **1602**. The B multiplexer **212** includes a Booth recode table **218** and a shift and complement unit **220**. The Booth recode table **218** receives inputs **224**, **226** from the two least significant bits of the S register and from a Booth register (S reg and Boothreg). Booth recoding is based on these inputs and the Booth recode table transforms these bits into shift, transport and invert control bits which are fed to the shift and complement unit **220**. The shift and complement unit **220** applies shift, transport and invert operations to the contents of the V register. The shift operation shifts the V register one bit to the left, shifting in a 0, and the transport and invert bits cause the possibly shifted result to be transported, inverted or zeroed or a combination of those.

FIG. **15** shows a block diagram of the alu **214** of the processor element shown in FIG. **13**. The alu **214** receives 10 bit inputs **234** from the A and B multiplexers **210** and **212**, and also receives inputs **244** and **246** from the BoothCarryIn and CarryReg registers. The alu **214** also receives instructions from the controller. The alu **214** includes a carry propagate unit **236**, a carry generate unit **238** and a carry select unit **242**. The alu also includes an exclusive OR (XOR) gate **250** for determining the alu result output. A CarryChain unit **240** receives inputs from Carry propagate unit **236** and the carry generate unit **238**, and outputs a result to the XOR gate **250**.

The various units in the alu **214** operate to carry out instructions issued by the controller.

The invention claimed is:

1. A method of retrieving a data item from a memory unit in a data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, wherein the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items and wherein the data processing apparatus includes said memory unit in which data items are stored at addresses therein, and to which the plurality of processing elements have access. the method comprising:

for each processing element in the array which requires access to the memory unit. setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

retrieving at least one data item stored at the transmitted target address in the memory unit;

transmitting the at least one retrieved data item and associated transaction identification information to the processing elements in the array; and

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, receiving the or each retrieved data item.

2. A method of writing data items to a memory unit in a data processing apparatus comprising a SIMD (single instruction multiple data) array of processing elements, wherein the processing elements are operably divided into a plurality of processing blocks, the processing blocks being operable to process respective groups of data items, and wherein the data processing apparatus includes the memory unit in which data items are stored at addresses therein, and to which the plurality of processing elements have access the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

selecting one of the processing elements having the access indicator set, and retrieving the stored target address from that selected processing element;

transmitting the retrieved target address and transaction identification information to all the processing elements in the array;

for each processing element having the access indicator set, comparing the transmitted target address with the stored target address, and if the stored and transmitted target addresses are equivalent, clearing the access indicator and storing the transaction identification information;

transmitting transaction identification information to the processing elements in the array;

for each processing element having stored transaction identification information, comparing the stored transaction identification information with the transmitted transaction identification information, and if the stored transaction information is equivalent to the transmitted transaction information, transmitting at least one data item to be stored in the memory unit at the target address; and

storing the at least one transmitted data item at the target address in the memory unit.

3. A method as claimed in claim **2**, wherein processing elements store data items at respective regions of the target memory address.

4. In a data processing apparatus, a method of retrieving a data item from a memory unit in which data items are stored at addresses therein, said data processing apparatus further comprising an array of a plurality of processing elements which have access to the memory unit, the method comprising:

for each processing element in the array which requires access to the memory unit, setting an access indicator to indicate that the processing element concerned requires access to the memory unit, and storing a target address of the memory unit to which such access is required;

Notice of Allowability	Application No.	Applicant(s)	
	09/972,797	STUTTARD ET AL.	
	Examiner	Art Unit	
	David J. Huisman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on July 20, 2007*.

2. ☒ The allowed claim(s) is/are *72-74 and 200-205 (hereafter renumbered as claims 1-9)*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☒ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: *all*.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date see attached.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Michael A. Glenn, Reg. No. 30,176, on August 24, 2007, and again on September 10, 2007.

The application has been amended as follows:

Amendments to the Claims

2. Regarding claim 72:

- In line 6, replace "a said memory unit" with --said memory unit--.
- In lines 7-8, delete "to the memory unit".
- In line 1 of paragraph 7 (beginning with "transmitting..."), replace "or each" with --at least one--.
- In the last two lines of the last paragraph, replace "or each" with --at least one--.

3. Regarding claim 73:

- In the 2nd to last line of the claim, replace "or each" with --at least one--.

4. Regarding claim 200:

- In line 1 of paragraph 7 (beginning with "transmitting the or each..."), replace "or each" with --at least one--.
- In the last two lines of the last paragraph, replace "or each" with --at least one--.

5. Regarding claim 203:

- In the 2nd to last line of the claim, replace "or each" with --at least one--.

Amendments to the Title

6. Per MPEP 606.01, please replace the current title with --Memory Access Consolidation for SIMD Processing Elements Having Access Indicators--.

Drawings

7. Regarding the drawings, now that the application has been allowed, please submit formal drawings, especially for Fig.13, which will be printed on the front of the patent upon issue.

Reasons For Allowance

8. The following is an examiner's statement of reasons for allowance:

Regarding claims 72 and 200, the prior art of record has failed to teach, both individually and in combination, and together with all additional claimed features, the consolidation of memory read accesses by having each processing element requiring memory access set an access indicator, selecting one of the access indicating elements, transmitting the selected one's target address to the remaining elements for comparison against target addresses of those indicating access and, for those elements that have a matching target address, clearing the indicator and storing ID information, retrieving the data item from memory at the selected one's target address, and receiving the data item by each processing element having the stored ID information.

Regarding claims 73 and 203, the prior art of record has failed to teach, both individually and in combination, and together with all additional claimed features, the consolidation of memory write accesses by having each processing element requiring memory access set an access indicator, selecting one of the access indicating elements, transmitting the selected one's target address to the remaining elements for comparison against target addresses of those indicating access and for those elements that have a matching target address, clearing the indicator and storing ID information, transmitting ID information and, for the set of elements having matching ID information, transmitting data from the set to be stored in memory at the target address.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DJH
David J. Huisman
September 10, 2007